

K

Notice of Allowability	Application No.	Applicant(s)
	09/471,244	BESHAI, MAGED E.
	Examiner	Art Unit
	Joon H. Hwang	2162

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. This communication is responsive to a telephone interview with David Greer (Reg. No. 43,395) on 9/27/05.
2. The allowed claim(s) is/are 13,16-23,27,28,30-32,34-37 and 43 (renumbered as 1-19).
3. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All
 - b) Some*
 - c) None
 of the:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

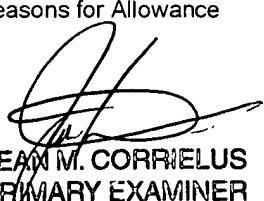
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) hereto or 2) to Paper No./Mail Date _____.
 - (b) including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. Notice of References Cited (PTO-892)
2. Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____
4. Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. Notice of Informal Patent Application (PTO-152)
6. Interview Summary (PTO-413),
Paper No./Mail Date _____
7. Examiner's Amendment/Comment
8. Examiner's Statement of Reasons for Allowance
9. Other _____.



JEAN M. CORRIEULUS
PRIMARY EXAMINER

DETAILED ACTION

1. The applicant amended claims 13, 16, 23, 27, 28, 30, 32, 36, and 37 and canceled claims 14-15, 24-26, 29, 33, and 42 in the amendment received on 9/15/05.

The pending claims are 13, 16-23, 27-28, 30-32, 34-37, and 43.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. Authorization for this examiner's amendment was given in a telephone interview with David Greer (Reg. No. 43,395) on 9/27/05 and Fraser D. Rowan (Reg. No. 53,870) on 9/30/05.

4. The application has been amended as follows:

Rewrite claim 13 as follows:

"13. A method of resolving B bit long addresses of packets into prefixes of any length up to B by a use of a data structure, wherein the data structure comprises a length sorted table Q and a plurality of secondary search units, table Q containing data related to prefixes of length not exceeding A, $A \leq B$ and each secondary search unit including tables V and T, wherein tables V and T are in one-to-one correspondence to one another and each comprising a $2 \times M$ memory, M being a positive integer, the method comprising steps of:

(1) indexing table Q by using first A bits of an address to generate a corresponding prefix of length equal to or less than A, or a pointer to a secondary search unit;

(2) accessing table V of the secondary search unit indicated by the pointer using each successive remaining bit of the address in order;

(3) accessing table T of the secondary search unit at each successive location corresponding to a location of table V accessed in step (2); and

(4) reading a valid data contained at a location in table T, the valid data being a prefix of length more than A,

wherein steps (2)-(4) are performed for at least two of said addresses in at least two of the secondary search units in parallel, and

wherein each secondary unit comprises one or more search branches and a pointer to a secondary search unit indicates an identity of the secondary unit and a branch number h, data relating to two or more search branches are interleaved in tables V and T of a secondary unit, and the method further comprises a step of accessing table V at a location indicated by the branch number h of the secondary unit identified by the pointer."

Rewrite claim 16 as follows:

"16. The method according to claim 13, wherein the step of accessing table V in each identified secondary search unit comprises further steps of:

- (5) accessing table V by using a first bit of the remaining bits of the address at a location identified by branch number h;
- (6) reading table V at a location indicating a next location of table V;
- (7) continue accessing and reading each successive location using each successive bit of the remaining bits until the Bth bit; and
- (8) continue reading the valid data contained at a location in table T corresponding to successive locations read in the step (7)."

Rewrite claim 17 as follows:

"17. The method according to claim 16, comprising further steps of:
accessing table T at a location corresponding to each successive location accessed in steps (5)-(7);
recording data contained at each accessed location of table T; and
reading the valid data contained at the latest previously accessed location if last accessed locations contained no valid data."

Rewrite claim 18 as follows:

"18. The method according to claim 17, wherein u_j is j^{th} bit of a B-bit received address, and the B-bit received address is known to belong to branch h, the steps of

accessing and reading table V and T in each secondary search unit are performed as follows to generate a prefix t:

```
y=h, t=0
for 1≤d≤B
{
    x=ud ;
    if (T(x, y) >0) t=T(x, y);
    y=V(x, y)
    if V(x, y) >0, y=V(x, y)
},
```

where y is an address-branch index and x is a bit-position in said B-bit received address."

Rewrite claim 19 as follows:

"19. The method according to claim 18, wherein the step of reading the valid data contained at the location in table T is replaced by steps of:

reading an indicator contained at the location in table T;
accessing a storage device at a location indicated by the indicator; and
reading the valid data contained at the location indicated by the indicator in the storage device."

Rewrite claim 20 as follows:

"20. The method according to claim 19, further comprising a step of:

scrambling all bits of the addresses to be translated according to a reproducible formula."

Rewrite claim 22 as follows:

"22. The method according to claim 13, wherein length sorted table Q provides an indication of '00' if an address cannot be resolved, "01" if a prefix is found, and "10", if a further search is required in a respective secondary search unit, wherein a "10" outcome is associated with a branch number."

Rewrite claim 23 as follows:

"23. An apparatus for address translation of a packet, comprising:

a parsing block for receiving the packet and parsing an address of the packet, the address having length B, B being a positive integer;

an indexing block for directly accessing a sorted prefix directory by first A binary bits, A<B, the sorted prefix directory containing translated prefixes of length not exceeding A and data specifying one of a plurality of secondary search units;

the plurality of secondary search units each having a secondary memory for searching in parallel for different prefixes of length greater than A; and

a scrambling unit for scrambling the first A bits of the address to be translated according to a reproducible formula,

wherein each secondary memory comprises tables V and T containing interleaved tree branches, each of said tree branches corresponding to an entry in said sorted prefix directory, and wherein each prefix of length longer than A belongs to a specific branch and each secondary memory contains prefixes of at least one branch."

Rewrite claim 27 as follows:

"27. The apparatus according to claim 23 wherein the reproducible formula is a bit reversal of the first A bits in the address."

Rewrite claim 28 as follows:

"28. An address translation apparatus for telecommunications networks, wherein packets are transported to addresses contained therein, comprising:

an address separation unit for separating from a packet an address to be translated;

primary translation unit having a primary translation table for translating the address to a prefix, the primary translation table containing prefixes, wherein widths of

the prefixes are less than a predetermined value and locations of branch search data structures in secondary search units;

 a plurality of secondary search units for performing secondary searches in parallel, each secondary search unit having a secondary memory storing a branch search data structure for performing each secondary search and translating the address to a prefix, if the primary translation table indicates a location of a branch search data structure to begin a secondary search; and

 an address scrambling unit for scrambling the address according to a predetermined reproducible formula."

Rewrite claim 31 as follows:

"31. The address translation apparatus according to claim 28 wherein said secondary searches are concurrently performed for a number of distinct addresses not exceeding a number of secondary search units in said plurality of secondary search units."

Rewrite claim 32 as follows:

"32. A method of translating addresses each comprising a prefix and a remaining part, said prefix having a respective unknown number of bits, the method comprising steps of:

defining an indexing part comprising a predetermined number of bits;
indexing a first memory device containing an indexing table based upon said
indexing part;

determining from said indexing a translation code, a first pointer, and a second
pointer;

said translation code is a first predetermined value or a second predetermined
value; and

if said translation code equals the first predetermined value,
accessing a secondary memory device from among a plurality of secondary
memory devices, said secondary memory device corresponding to said first pointer and
storing a plurality of prefixes encoded in at least one tree structure;

performing a tree-search process on one of said at least one tree structure
having a root defined by said second pointer, wherein said tree-search process
identifies the prefix; and

equating the prefix to a word comprising concatenation of said first pointer and
said second pointer if said translation code comprises the second predetermined value."

Rewrite claim 36 as follows:

"36. A method of translating addresses each comprising a prefix and a remaining part, said prefix having a respective unknown number of bits, the method comprising steps of:

defining an indexing part comprising a predetermined number of bits;

indexing a first memory device containing an indexing table based upon said indexing part;

determining from said indexing a translation code, a first pointer, and a second pointer, wherein said translation code equals a predetermined value;

accessing a secondary memory device from among a plurality of secondary memory devices, said secondary memory device corresponding to said first pointer and storing a plurality of prefixes encoded in at least one tree structure; and

performing a tree-search process on one of said at least one tree structure having a root defined by said second pointer, wherein said tree-search process identifies the prefix,

wherein said steps of indexing, determining, and accessing are executed in a sequential temporal order and said tree-search process for one of said addresses is performed concurrently with said tree-search process for at least one other of said addresses in at least two of said secondary memory devices, and

buffering said second pointer at said secondary memory device if said secondary memory device is in use in said tree-search process for another one of said addresses."

Rewrite claim 37 as follows:

"37. A method of resolving addresses comprising steps of:

receiving a multiplicity of addresses, each address including a first prefix of unknown length;

indexing, using a fixed part of said each address, an indexing table Q, to read a translation code and data record;

said translation code is a first predetermined value, a second predetermined value, or a third predetermined value;

resolving said data record as a translation if said translation code equals the first predetermined value;

resolving said data record to two identifiers if said translation code equals the second predetermined value, a first of said two identifiers indicating a target secondary search unit in a plurality of secondary search units and a second of said two identifiers indicating a location in said target secondary search unit, wherein the location corresponds to a root of a branch, said branch comprising prefixes having in common said fixed part of said each address; and

resolving said each address as unknown if said translation code equals the third predetermined value,

wherein said each address, excluding said fixed part of said each address, is further processed by said target secondary search unit to resolve said each address to a translation, wherein at least two of said secondary search units concurrently process at least two addresses in said multiplicity of addresses, and wherein at least one of said addresses in said multiplicity of addresses is queued in a buffer associated with said target secondary unit."

Allowable Subject Matter

5. Claims 13, 16-23, 27-28, 30-32, 34-37, and 43 are allowed.

Reason For Indicating Allowable Subject Matter

6. Claims 13, 23, 28, 32, 36, and 37 identify the distinct features, "(1) indexing table Q by using first A bits of an address to generate a corresponding prefix of length equal to or less than A, or a pointer to a secondary search unit; (2) accessing table V of the secondary search unit indicated by the pointer using each successive remaining bit of the address in order; (3) accessing table T of the secondary search unit at each successive location corresponding to a location of table V accessed in step (2); and (4) reading a valid data contained at a location in table T, the valid data being a prefix of length more than A, wherein steps (2)-(4) are performed for at least two of said addresses in at least two of the secondary search units in parallel, and wherein each secondary unit comprises one or more search branches and a pointer to a secondary search unit indicates an identity of the secondary unit and a branch number h, data

relating to two or more search branches are interleaved in tables V and T of a secondary unit, and the method further comprises a step of accessing table V at a location indicated by the branch number h of the secondary unit identified by the pointer." for claim 13, "a parsing block for receiving the packet and parsing an address of the packet, the address having length B , B being a positive integer; an indexing block for directly accessing a sorted prefix directory by first A binary bits, $A < B$, the sorted prefix directory containing translated prefixes of length not exceeding A and data specifying one of a plurality of secondary search units; the plurality of secondary search units each having a secondary memory for searching in parallel for different prefixes of length greater than A ; and a scrambling unit for scrambling the first A bits of the address to be translated according to a reproducible formula, wherein each secondary memory comprises tables V and T containing interleaved tree branches, each of said tree branches corresponding to an entry in said sorted prefix directory, and wherein each prefix of length longer than A belongs to a specific branch and each secondary memory contains prefixes of at least one branch." for claim 23, "an address separation unit for separating from a packet an address to be translated; primary translation unit having a primary translation table stored in a memory for translating the address to a prefix, the primary translation table containing prefixes, wherein widths of the prefixes are less than a predetermined value and locations of branch search data structures in secondary search units; a plurality of secondary search units for performing secondary searches in parallel, each secondary search unit having a secondary memory storing a branch search data structure for performing each secondary search and translating the address

to a prefix, if the primary translation table indicates a location of a branch search data structure to begin a secondary search; and an address scrambling unit for scrambling the address according to a predetermined reproducible formula." for claim 28, "defining an indexing part comprising a predetermined number of bits; indexing a first memory device containing an indexing table based upon said indexing part; determining from said indexing a translation code, a first pointer, and a second pointer; said translation code is a first predetermined value or a second predetermined value; if said translation code equals the first predetermined value, accessing a secondary memory device from among a plurality of secondary memory devices, said secondary memory device corresponding to said first pointer and storing a plurality of prefixes encoded in at least one tree structure; performing a tree-search process on one of said at least one tree structure having a root defined by said second pointer, wherein said tree-search process identifies the prefix; and equating the prefix to a word comprising concatenation of said first pointer and said second pointer if said translation code comprises the second predetermined value." for claim 32, "defining an indexing part comprising a predetermined number of bits; indexing a first memory device containing an indexing table based upon said indexing part; determining from said indexing a translation code, a first pointer, and a second pointer, wherein said translation code equals a predetermined value; accessing a secondary memory device from among a plurality of secondary memory devices, said secondary memory device corresponding to said first pointer and storing a plurality of prefixes encoded in at least one tree structure; and performing a tree-search process on one of said at least one tree structure having a root

defined by said second pointer, wherein said tree-search process identifies the prefix, wherein said steps of indexing, determining, and accessing are executed in a sequential temporal order and said tree-search process for one of said addresses is performed concurrently with said tree-search process for at least one other of said addresses in at least two of said secondary memory devices, and buffering said second pointer at said secondary memory device if said secondary memory device is in use in said tree-search process for another one of said addresses." for claim 36, and "receiving a multiplicity of addresses, each address including a first prefix of unknown length; indexing, using a fixed part of said each address, an indexing table Q, to read a translation code and data record; said translation code is a first predetermined value, a second predetermined value, or a third predetermined value; resolving said data record as a translation if said translation code equals the first predetermined value; resolving said data record to two identifiers if said translation code equals the second predetermined value, a first of said two identifiers indicating a target secondary search unit in a plurality of secondary search units and a second of said two identifiers indicating a location in said target secondary search unit, wherein the location corresponds to a root of a branch, said branch comprising prefixes having in common said fixed part of said each address; and resolving said each address as unknown if said translation code equals the third predetermined value, wherein said each address, excluding said fixed part of said each address, is further processed by said target secondary search unit to resolve said each address to a translation, wherein at least two of said secondary search units concurrently process at least two addresses in said multiplicity of addresses, and

wherein at least one of said addresses in said multiplicity of addresses is queued in a buffer associated with said target secondary unit." for claim 37, are not taught or suggested by the prior art made of records. The closest prior art, Lampson et al. ("IP Lookups using Multiway and Multicolumn Search", 1998, IEEE, pages 1248-1256) disclosing IP address lookup by searching and matching prefix of an IP address, fails to suggest the claimed limitations as mentioned above in combination with other claimed elements. The above features in conjunction with all other limitations of the dependent and independent claims 13, 16-23, 27-28, 30-32, 34-37, and 43 are hereby allowed.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joon H. Hwang whose telephone number is 571-272-4036. The examiner can normally be reached on 9:30-6:00(M~F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JOHN E. BREENE can be reached on 571-272-4107. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joon Hwang
Patent Examiner
Technology Center 2100

9/30/05



JEAN M. CORRELUS
PRIMARY EXAMINER